Adiabatic Digital Circuits Based on Sub-threshold Operation of Pass-transistor and Slowly Ramping Signals

Aleksandar Pajkanović, Tom J Kazmierski, Branko Dokić

Abstract - An overview of pass-transistor logic and subthreshold operation of transistors is given in this paper. Benefits of combining these two design principles from overall energy consumption point of view are discussed. A simulation to prove extremely low supply voltage and low power consumption operation of thus designed digital circuits is performed. The results obtained imply that it is possible to preserve energy by slowing down transitions between input signal logic levels.

Keywords – pass-transistor logic, sub-threshold operation, low power consumption, energy efficiency, energy harvesters.

I. Introduction

Logic circuits in standard applications are optimized in such way that their operation yields minimum delay. The operation point which is targeted in such optimization is known as the minimum-delay operation point (MDP). Since minimum delay means maximum speed and maximum speed implies maximum power consumption, it is not possible to use this approach when energy efficiency is an issue. This issue appeared with the emergence of the applications that require ultralow energy levels, such as energy-harvester powered wireless sensors. In such systems the energy consumption, rather than speed, is the most important design concern. In order to address the energy concern, the opposite of MDP, i.e. the minimum-energy operation point (MEP) also became a very interesting part of the energy-delay space. This has led to a completely changed design approach: to design a circuit with the power consumption minimized, initial design point is MEP, not MDP [1].

It is well known that MEP occurs in the sub-threshold operational region of the MOS transistors and that its value is set by leakage [1]. The operation at MEP has been demonstrated and proven to be possible [2]. Of course, as there were disadvantages in operating at MDP, there are some when operating at MEP. The delay at MEP is at least three orders of magnitude larger than at MDP, as illustrated in Fig. 1. Besides, sub-threshold logic has to be ratioed to be functional and sensitivity to parameter variance is increased in the weak inversion area [1].

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Ever since the pass-transistor logic (PTL) was introduced over two decades ago by K. Yano in his papers (e.g. [3]), this technology was sure to yield improvement on the field of power consumption, speed and area when logic circuits are in question [4]. The main concept behind PTL is the utilization of nMOS pass-transistor network for logic organization, instead of source-grounded nMOS trees in the conventional differential logic. The main reason that PTL achieves higher speed and lower power dissipation is that its input capacitance is about half that of the conventional CMOS configuration. Also, PTL is able to realize complex Boolean functions efficiently in a small number of MOS transistors, thus reducing the area and delay time [3]. The first design methodology intended for PTL was introduced by Yano e.a. [4], thus solving the most important reason for PTL not being able to capture a major role within logic circuits design.

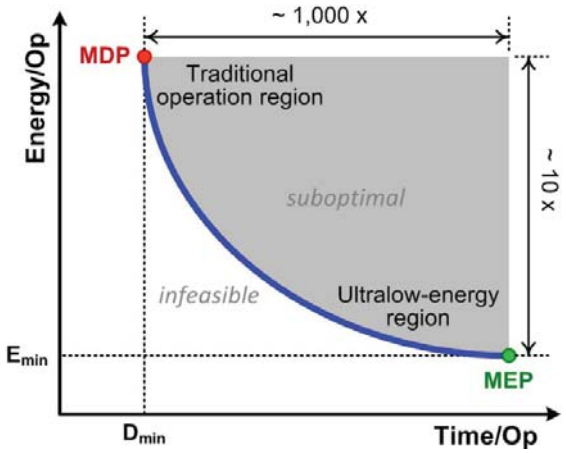

Fig. 1. Energy-delay space, MDP and MEP marked [1].

It has also been pointed out [5] that all previous researches on PTL examine the behaviour of full-adders. In that paper it is claimed that a full-adder structure is very easy to design using any of PTL approaches and is the least efficient structure for CMOS. Also, it is said that PTL styles have difficult layout and require greater design efforts. These conclusions come from the claim that CMOS is the most widespread logic style at the point of time. Since [5] has been published almost fifteen years ago, there

is no reason to oversee all the other aforementioned advantages of PTL [6].

Two different approaches for minimising energy consumption have been mentioned until now. Each of these has been subject of many different papers, thus they are both very thoroughly covered in literature, but their combination is not. Since PTL is considered low power logic, operating it in sub-threshold region, which implies extremely low energy consumption, would yield an ultralow power digital system. Because of the minimal voltage supply (a condition to operate in sub-threshold region), such circuits would have limited performance in terms of speed. They would therefore be suitable for applications where performance is not of primary importance, such as energy harvester applications. Namely, the conventional method uses a general purpose MCU with performance capabilities much more advanced than what the system requires. These MCUs are able to work in a wide range of higher clock frequencies, they have many fast and accurate input/output peripherals and terminals. In contrast to the above mentioned standard MCUs, in energy harvester applications more energy efficient circuits and modes of operation are required. These conditions are to be yielded by the combination of the following two design methods: PTL and sub-threshold operation. Thus, two main benefits for energy harvesters would arise: very low voltage supply and ultralow power consumption of the system [6].

In this paper a simulation of PTL digital circuits operating in sub-threshold region is performed. Throughout the simulation the rise and fall time intervals of the input voltage are varied, thus slowing down the change of the input voltage from one logic level to the other. The results of the simulation showed that the power consumption decreases as the rise and fall time intervals increase until a certain point where it reaches its minimum. Afterwards, power consumption increases again. Thus, in order to preserve energy, changes of the input voltage should be slower.

To the authors' knowledge, accept for [6], the literature on PTL operating in sub-threshold region is very scarce.

The rest of the paper is structured as follows. In sections II and III short overviews of operation in sub-threshold region and PTL are given, respectfully. Section IV presents the performed simulation and the results thusly obtained. In section V the results are discussed.

II. Operation in Sub-Threshold Region

When operating in a standard set-up, a MOSFET has the gate voltage greater than the threshold voltage, $V_{gs} > V_T$. This is operation in strong inversion region. Ideally, for $V_{gs} < V_T$ MOSFETs do not conduct current. However, there is a number of carriers which create a current between drain and source. Thus, MOSFET is in the weak inversion region, because the inversion layer of carriers is not yet formed. This region is also known as the sub-threshold region of operation [7].

In the sub-threshold region the gate current is negligible relative to the sub-threshold current because it decreases much faster with V_{DD}. Other leakage components such as the gate induced drain leakage and pn-junction leakage are also negligible in sub-threshold. Thus, the following analysis justifiably equates the total current to the sub-threshold current for V_{DD} in the sub-threshold region [7]:

$$I_{sub} = I_0 e^{\frac{V_{gs}-V_t}{n\varphi_t}}, \tag{1}$$

$$I_0 = \mu_0 C_{ox} \frac{W}{L}(n-1)\varphi_t^2, \tag{2}$$

where n is the sub-threshold slope factor ($1+C_d/C_{ox}$) and φ_t is kT/q.

An equally important parameter is the delay of logic gates. Eq. (3) shows the propagation delay of a characteristic inverter with the output capacitance C_g in sub-threshold [7]:

$$t_d = \frac{KC_g V_{DD}}{I_{o,g} e^{\frac{V_{gs}-V_{t,g}}{n\varphi_t}}} \tag{3}$$

where K is a delay fitting parameter. The expression for the current in the denominator of Eq. (3) models the *on* current of the characteristic inverter, so it accounts for transitions through both nMOS and pMOS devices. Unless the pMOS and nMOS are perfectly symmetrical, the terms $I_{o,g}$ and $V_{T,g}$ are fitting parameters that do not correspond exactly with the MOSFET parameters of the same name [7].

The operational frequency is simply [7]:

$$f = \frac{1}{t_d L_{DP}} \tag{4}$$

where L_{DP} is the depth of the critical path in characteristic inverter delays [7].

A mathematical model for the total energy consumption per cycle is further developed [7], yielding expressions for calculation of the optimum supply voltage and optimum threshold voltage for a given performance condition – frequency. These expressions are [7]:

$$V_{DDopt} = n\,\varphi_t[2 - lambertW(\beta)] \tag{5}$$

$$V_{Topt} = V_{DDopt} - n\varphi_t ln\left(\frac{fKC_g L_{DP} V_{DDopt}}{I_{o,g}}\right) \tag{6}$$

where:

$$\beta = \frac{-2C_{eff} e^2}{W_{eff} L_{DP} KC_g} > -\frac{1}{e}; \tag{7}$$

C_{eff} is the average effective switched capacitance of the entire circuit, including the average activity factor over all of its nodes; W_{eff} estimates the average total width relative to the characteristic inverter; Lambert W function gives the solution to the equation $We^W = x$ [7].

The constraint given by Eq. (7) shows that there is a maximum achievable frequency for a given circuit in the sub-threshold region [7].

A way to even more improve energy efficiency while operating in sub-threshold region is described in [8]. Namely, dynamic threshold MOS (DTMOS) technique and its advantages and disadvantages are shown in this paper. Using this technique, the transistor threshold becomes dependent on the gate voltage – because gate is connected to the body. Thus, low leakage ($V_g = V_b = 0 \rightarrow V_T$ high) and high drive ($V_g = V_b = V_{DD} \rightarrow V_T$ low) are obtained. In the paper it is demonstrated that DTMOS can be used for a broad range of supply voltages. DTMOS delay and efficiency are superior to traditional designs as the voltage is reduced and the loading is increased. A drawback of this technique is that it is limited to 0.5V supply voltage, because forward biasing the source-body pn junction would lead to excessive gate current. Also, the problems that appear are area penalty and process complexity [8].

III. PASS-TRANSISTOR LOGIC

In contrast to classic static CMOS logic, in PTL two input logic signals are applied at the gate and at the drain of a MOS transistor, as shown in Fig. 2. Considering an ideal case, without load, the transistor shown in Fig. 2 is saturated when its gate and drain voltages are equal to V_{DD}. Thus, the source voltage is V_{DD}-V_T. However, the source will be in high impedance state for 0V gate voltage, no matter what the drain voltage is. Therefore, another nMOS is added and sources are connected to a single node to ensure that the logic function is valid for both values of B. This is illustrated in Fig. 3. This is an effective method to realize the logic AND function, because it requires only two nMOS transistors, whereas classic static CMOS would use six transistors. Additionally, it is possible to alter the logic function of the circuit only by changing the wiring of the input signals [6].

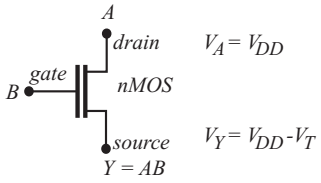

Fig. 2. NMOS transistor operating as pass-transistor.

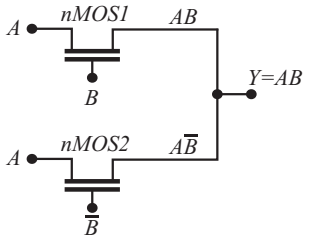

Fig. 3. Two nMOS transistors creating logic function AND.

A significant disadvantage of PTL is that the output voltage is lower than the input and that it does not allow series connections of large numbers of transistors. The addition of a static inverter, Fig. 4, recovers the voltage swing to appropriate values [6].

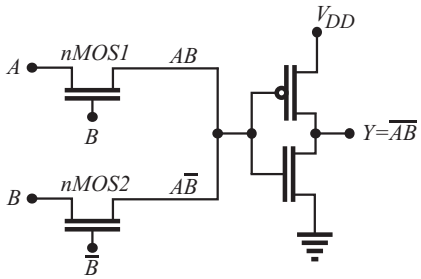

Fig. 4. Voltage swing recovery with static inverter.

There have been several different approaches to PTL design, some of which are: complementary pass-transistor logic (CPL), double pass-transistor logic (DPL) and dual value logic (DVL). All of these have their advantages and disadvantages, but CPL will be used within this paper, since it has been shown to result in high speed and high logic functionality [9].

CPL consists of complementary input/output, nMOS pass-transistor logic network and CMOS output inverters. A pMOS latch can also be added to CPL, as shown in Fig. 5, in order to decrease static power consumption and return the full swing [10]. Arbitrary Boolean functions can be constructed from the pass-transistor network by combining four basic circuit modules: AND/NAND, OR/NOR, XOR/XNOR and a wired-AND/NAND module [3].

There have been reports [11-13] which prove the functionality of CPL. The results shown in these papers justify the usage of CPL since it is said that the effect of parasitic capacitances is decreased [11] and delays can be reduced by 30% [12]. Circuit synthesis is possible using multiplexers and inverter only as components of the PTL cell library [13].

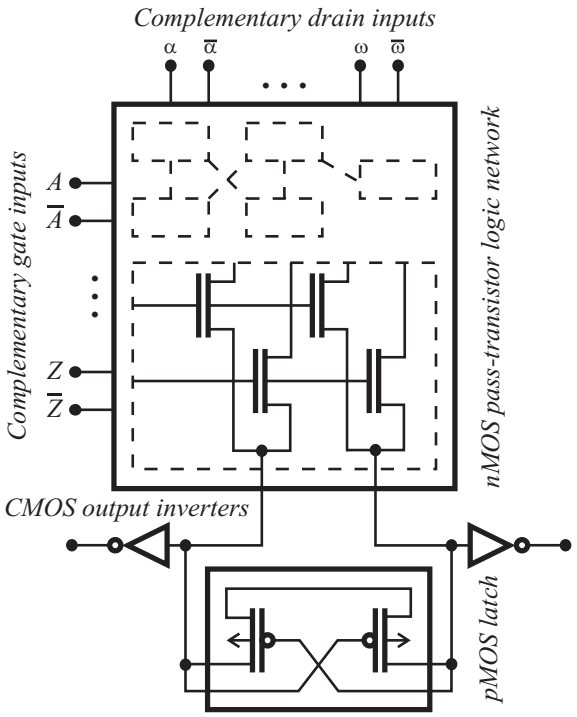

Fig. 5. Basic circuit configuration in CPL [3].

IV. Simulation Results

In order to show the influence of the input signal switching speed on the behaviour of PTL operating in sub-threshold region concerning power consumption, a set of simulations have been performed and are presented in this paper.

Two digital circuits designed using aforementioned low-power principles have been simulated – a NAND gate and a full-adder. For both of these the supply voltage is V_{DD} = 0.3V. The NAND circuit was simulated as shown in Fig. 4 and full-adder was simulated as shown by Ivanov [6]. MOSFET models used in these simulations are BSIM3 and the technology process is 130nm. The BSIM model shows good physical behaviour in the sub-threshold region [14]. Since Ivanov [6] uses MOSFET models of a 350nm technology process, in this paper the channel widths are scaled down proportionally. Throughout the simulations all the inputs, for both circuits, are short-circuited since the input voltage set-up causes a logic state change at the output for every clock interval. Thus, the worst power consumption case is observed. In order to obtain more accurate results, a simulation was performed over one hundred cycles of the clock signal. The power consumption is calculated as:

$$W = V_{DD} \cdot \int i_{DD}(t)\, dt. \tag{8}$$

Since this is the power consumed over one hundered cycles, the power per cycle is given as:

$$W_{pc} = W / 100. \tag{9}$$

Throughout the simulations the rise, fall, high and low intervals of the input signal are as follows. The rise interval t_r is defined as the time that the input signal takes to change between logic zero to logic one. The fall interval t_f is the time taken to change from logic one to logic zero. The high interval t_h is the time during which logic one is held at the input and during the low interval t_l logic zero is held. The interval values for which the simulations were carried out are:

$$t_h = t_l = \{5, 50, 500\}\ [\mu s] \text{ and}$$

$$t_r = t_f = \{0, 10, 20, 50, 100, 200, 500, 1000\}\ [ns].$$

All the combinations of the two listed sets were simulated and the results are shown in Fig. 6 and Fig. 7 for the NAND circuit and the full-adder, respectively.

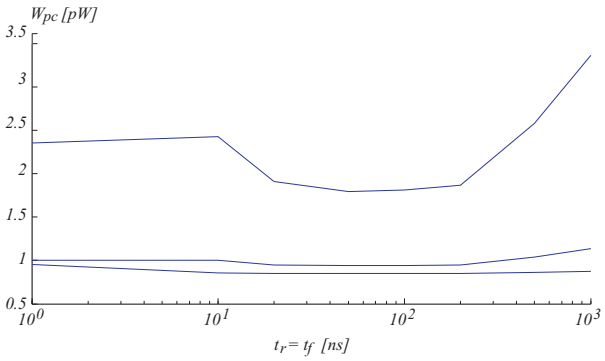

Fig. 6. Dependence of power consumption of sub-threshold PTL NAND circuit on rise and fall time of input signal.

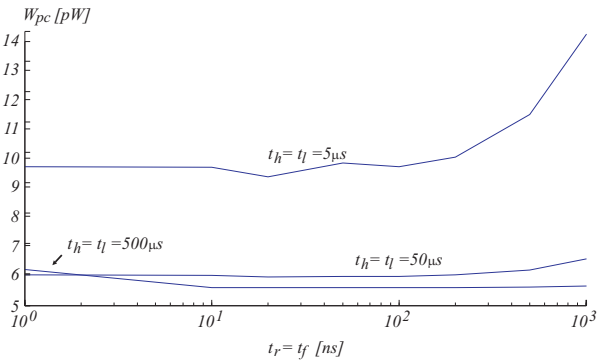

Fig. 7. Dependence of power consumption of sub-threshold PTL full-adder circuit on rise and fall time of input signal.

In Table I the rise and fall intervals at which the minimum power consumption is reached and the percentage reduction achieved relative to the instantaneous switching are shown.

TABLE I
MINIMUM POWER CONSUMPTION ACHIEVED

	NAND		full-adder	
$t_h = t_l$ [µs]	$t_{rmin} = t_{fmin}$ [ns]	power saved [%]	$t_{rmin} = t_{fmin}$ [ns]	power saved [%]
5	50	15.84	20	3.71
50	50	6.05	20	1.35
500	50	31.57	50	30.15

Simulation files are available at the authors' webpage[1].

V. DISCUSSION

The static component of the transistor sub-threshold current is given by eq. (1). Since this current does not depend on the input voltage rise and fall time intervals, from the results obtained in section IV it is obvious that through the supply voltage source, there exists another component of the sub-threshold current, namely the dynamic component. This current, I_{dyn}, is explained as the influence of the parasitic capacitances during the transition periods t_r and t_f. The capacitances which are greatly responsible for this current are shown in Fig. 8.

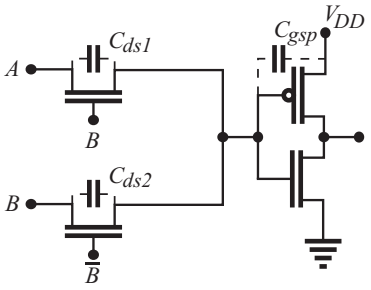

Fig. 8. Capacitances through which I_{dyn} flows.

Since $C_{gsp} << C_{dsp}$, the dynamic current flows for a shorter time than that for the current that flows through the output inverter, obtained from (1) and expressed as [10]:

$$I_{static} = I_{sp} = I_{sn} = I_0 e^{\frac{V_{gsn}-V_{tn}}{n\varphi_t}} = I_0 e^{\frac{V_{gsp}-V_{tp}}{n\varphi_t}}. \quad (10)$$

Also, the equation that describes dynamic component is dervided as:

$$I_{dyn} = f\left(C\cdot\left(\frac{du}{dt}\right)\right). \quad (11)$$

Further, the power consumed by the flow of this current is as:

$$W_{dyn} = V_{DD}\frac{1}{t_r}\int_0^{t_r} f\left[C\cdot\left(\frac{du}{dt}\right)\right]dt, \quad (12)$$

where C represents the effective capacitance of the whole circuit given in Fig. 8, and u is the voltage over this capacitance. An analogous equation can be derived for the input voltage fall time interval.

From eq. (12) it is obvious that the dynamic current decreases as time interval, during which the voltage difference appears, increases. However, this decrease in power consumption by increasing the time intervals of switching levels can happen only to a certain point. Namely, at the same time as the average value of I_{static} increases the above mentioned time intervals increase. With this increase, I_{static} becomes the dominant component, thus disabling further power consumption decrease.

Even though a concrete equation which utterly explains the dynamic component is not given in this paper, the previous discussion explains the behaviour of the power consumption shown if Figs. 6 and 7. At first, while I_{dyn} is dominant, the power consumption decreases with the increase of the switching time intervals. It reaches a minimum; and, when I_{static} becomes greater, it starts to increase.

VI. CONCLUSION

A summary of PTL and subthreshold ultralow energy operation has been given in this paper. Within sections II and III the advantages and disadvantages of these technologies have been described. Benefits of combining these two low power consumption design approaches have been pointed out.

Through a simulation of digital circuits based on sub-threshold operation of PTL it has been proven that this combination of technologies yields a very low energy consumption system. Also, according to the simulation results, it is possible to decrease the energy consumption by slowing down the switching time of logic levels at the system input. In other words, if the rise and fall time intervals are increased, the dynamic component of the supply voltage current is decreased, thus lowering the energy consumption. These results are shown in section IV, and discussed and explained in section V.

In future work, more detailed measurements will be made so that the presented effects can be further examined. Also, a detailed mathematical model for the dynamic component will be developed.

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